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Jack L. Lo, Joel S. Emer, Henry M. Levy, Rebecca L. Stamm, Dean M. Tullsen, S. J. Eggers
 August 1997 **ACM Transactions on Computer Systems (TOCS)**, Volume 15 Issue 3

Full text available:  pdf(526.39 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#), [review](#)

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Keywords: cache interference, instruction-level parallelism, multiprocessors, multithreading, simultaneous multithreading, thread-level parallelism

2 A new guaranteed heuristic for the software pipelining problem 

Pierre-Yves Calland, Alain Darte, Yves Robert
 January 1996 **Proceedings of the 10th international conference on Supercomputing**

Full text available:  pdf(892.93 KB) Additional Information: [full citation](#), [references](#), [index terms](#)

Keywords: circuit retiming, cyclic scheduling, guaranteed heuristic, list scheduling, software pipelining

3 AlphaSort: a RISC machine sort 

Chris Nyberg, Tom Barclay, Zarka Cvetanovic, Jim Gray, Dave Lomet
 May 1994 **ACM SIGMOD Record , Proceedings of the 1994 ACM SIGMOD international conference on Management of data**, Volume 23 Issue 2

Full text available:  pdf(1.17 MB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

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6 Implementation of a parallel unstructured Euler solver on shared and distributed memory architectures

D. J. Mavriplis, R. Das, R. E. Vermeland, J. Saltz

December 1992 **Proceedings of the 1992 ACM/IEEE conference on Supercomputing**

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7 GI-cube: an architecture for volumetric global illumination and rendering

Frank Dachille, Arie Kaufman

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Keywords: hardware accelerator, volume processing, volume rendering, volumetric global illumination, volumetric ray tracing

- 8 A compilation-based software estimation scheme for hardware/software co-simulation**
- Marcello Lajolo, Mihai Lazarescu, Alberto Sangiovanni-Vincentelli
March 1999 Proceedings of the seventh international workshop on Hardware/software codesign

Full text available: [pdf\(437.23 KB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

Keywords: compilation, delay modeling, software estimation

- 9 Application restructuring and performance portability on shared virtual memory and hardware-coherent multiprocessors**

Dongming Jiang, Hongzhang Shan, Jaswinder Pal Singh
June 1997 ACM SIGPLAN Notices , Proceedings of the sixth ACM SIGPLAN symposium on Principles and practice of parallel programming, Volume 32 Issue 7

Full text available: [pdf\(1.59 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

The performance portability of parallel programs across a wide range of emerging coherent shared address space systems is not well understood. Programs that run well on efficient, hardware cache-coherent systems often do not perform well on less optimal or more commodity-based communication architectures. This paper studies this issue of performance portability, with the commodity communication architecture of interest being page-grained shared virtual memory. We begin with applications that per ...

- 10 Compile/run-time support for threaded MPI execution on multiprogrammed shared memory machines**

Hong Tang, Kai Shen, Tao Yang
May 1999 ACM SIGPLAN Notices , Proceedings of the seventh ACM SIGPLAN symposium on Principles and practice of parallel programming, Volume 34 Issue 8

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- 11 The Totem multiple-ring ordering and topology maintenance protocol**

D. A. Agarwal, L. E. Moser, P. M. Melliar-Smith, R. K. Budhia
May 1998 ACM Transactions on Computer Systems (TOCS), Volume 16 Issue 2

Full text available: [pdf\(367.16 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#), [review](#)

The Totem multiple-ring protocol provides reliable totally ordered delivery of messages across multiple local-area networks interconnected by gateways. This consistent message order is maintained in the presence of network partitioning and remerging, and of processor failure and recovery. The protocol provides accurate topology change information as part of the global total order of messages. It addresses the issue of scalability and achieves a latency that increases logarithmically with ...

Keywords: Lamport timestamp, network partitioning, reliable delivery, topology maintenance, total ordering, virtual synchrony

12 A flexible operation execution model for shared distributed objects

Saniya Ben Hassen, Irina Athanasiu, Henri E. Bal

October 1996 **ACM SIGPLAN Notices , Proceedings of the 11th ACM SIGPLAN conference on Object-oriented programming, systems, languages, and applications**, Volume 31 Issue 10Full text available: [pdf\(2.30 MB\)](#)Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Many parallel and distributed programming models are based on some form of shared objects, which may be represented in various ways (e.g., single-copy, replicated, and partitioned objects). Also, many different operation execution strategies have been designed for each representation. In programming systems that use multiple representations integrated in a single object model, one way to provide multiple execution strategies is to implement each strategy independently from the others. How ...

13 Session 4: communications libraries: SLICC: a low latency interface for collective communications

Allan D. Knies, William J. Harrod, F. Ray Barriuso, George B. Adams

November 1994 **Proceedings of the 1994 ACM/IEEE conference on Supercomputing**Full text available: [pdf\(658.77 KB\)](#)Additional Information: [full citation](#), [abstract](#), [references](#)

Several recent parallel computers have implemented logically shared, physically distributed memory systems which allow processors to directly access memory in other processors without interrupting the referenced PE. Because this kind of architecture provides greater flexibility for interprocessor communications than private address space computers, different software models can be developed to take advantage of these machines. In this paper, we describe a low-level collective communications interface ...

14 Generalized FLP impossibility result for t-resilient asynchronous computations

Elizabeth Borowsky, Eli Gafni

June 1993 **Proceedings of the twenty-fifth annual ACM symposium on Theory of computing**Full text available: [pdf\(980.66 KB\)](#)Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)**15 High performance data mining (tutorial PM-3)**

Vipin Kumar, Mohammed Zaki

August 2000 **Tutorial notes of the sixth ACM SIGKDD international conference on Knowledge discovery and data mining**Full text available: [pdf\(8.06 MB\)](#)Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)**16 High performance synchronization algorithms for multiprogrammed multiprocessors**

Robert W. Wisniewski, Leonidas I. Kontothanassis, Michael L. Scott

August 1995 **ACM SIGPLAN Notices , Proceedings of the fifth ACM SIGPLAN symposium on Principles and practice of parallel programming**, Volume 30 Issue 8Full text available: [pdf\(915.40 KB\)](#)Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

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17 Communication and computation performance of the CM-5

T. T. Kwan, B. K. Totty, D. A. Reed

December 1993 **Proceedings of the 1993 ACM/IEEE conference on Supercomputing**

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18 An execution model for distributed object-oriented computation

Edward H. Bensley, Thomas J. Brando, Myra Jean Prelle

January 1988 **ACM SIGPLAN Notices , Conference proceedings on Object-oriented programming systems, languages and applications**, Volume 23 Issue 11

Full text available:  pdf(786.18 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)



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19 Totem: a fault-tolerant multicast group communication system

L. E. Moser, P. M. Melliar-Smith, D. A. Agarwal, R. K. Budhia, C. A. Lingley-Papadopoulos
April 1996 **Communications of the ACM**, Volume 39 Issue 4

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20 Model refinement for hardware-software codesign

Jie Gong, Daniel D. Gajski, Smita Bakshi

January 1997 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 2 Issue 1

Full text available:  pdf(436.53 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#), [review](#)



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Keywords: functional model, implementation model, model refinement, sofware-hardware codesign

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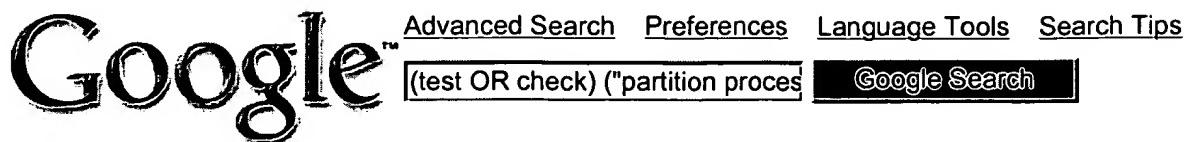
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... Beginning with V4R5, the **check** will be performed across ... The Details Shared Processor

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10ms ...

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... slightly more 5250 capacity than the **partition's processor** capacity (Note: LPAR would not ... Permanent: **Check** the field at offset 0x38, to determine how ...

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... z/VM is running in a logical **partition**) **processors** available to ... This capability can be extremely useful to **test** a guest ... z/VM is running in an **LPAR**, the logical ...

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... to meet the receiver value **test**, the next ... intervals Because adjusting logical **partition processor** weights can ... usage is understood by the **LPAR** cluster members ...

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... allow for dynamic adjustment of logical **partition processor** weights ... relevant to WLM involvement in IRD **LPAR** CPU management ... to pass the receiver value **test** and is ...

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... three (3) weeks to allow the Field Security Operations SRR team to **complete** its data ... Reference: **LPAR STIG 4.2.1.1** ... **Check** to see that a log exists and is used. ...

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... conditions is shown which were necessary to **complete** one SSCH ... TIME: 21.00.01 ACT:

POR MODE: **LPAR CPMF: EXTENDED** ... delivering up to 100 MB/sec, **full-duplex** data ...

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... No. 1 0.4 shared processor 64MB memory No direct attach I/O Linux SECONDARY No.2 0.5

shared processor 100MB memory 1 Gbit Ethernet IOA **LPAR** Validation Tool (LVT ...

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... Up to 32 partitions **LPAR** on Selected ... processing units: Number of **partition processors**:

Partial Processors ... CPW Avail) / 1000 (1 **partition processor**) = .50 or 50 ...

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... on the control panel (key in **manual** position) 2 ... job doing 5250 OLTP processing) **LPAR**

does impose ... more 5250 capacity than the **partition's processor** capacity (Note ...

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... by the machine's Logical Partitioning (**LPAR**) support to ... This **manual** also describes

the z/VM facilities ... running in a logical **partition**) **processors** available to ...

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... 6 DBLINX Number of **partition processors** Press F10 to IPL the **whole** system now ... F3=Exit

F10=IPL system to activate changes F12=Cancel Some **LPAR** Config Changes ...

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... Finally, no system discussion would be **complete** without some ... Logical Storage Unit, FXU = Fixed point (**integer**) Unit, BXU ... to the module, and the **full** L2 onboard ...

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... Logical Partition Environment The following is a brief explanation of the **LPAR** macro parameters. For more details see the SNAP/SHOT Input Reference Manual (S/S ...

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... business goals, WLM continuously adapts systems resources within an **LPAR** to actual ... parallel, thus reducing the overall elapsed time for the query to **complete** ...

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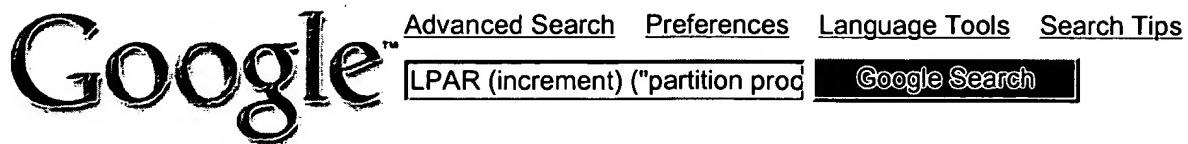
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